FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER
TRANSMITTAL LETTER TO THE UNITED STATES	PF980052
DESIGNATED/ELECTED OFFICE (DO/EO/US)	U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR
CONCERNING A FILING UNDER 35 U.S.C. 371	09/744796

INTERNATIONAL APPLICATION NO. PCT/FR99/01768	INTERNATIONAL FILING DATE 20July1999(20.07.99)	PRIORITY DATE CLAIMED 30July1998(30.07.98)

TITLE OF INVENTION

CLOCK RECOVERY METHOD IN DIGITAL SIGNAL SAMPLING

APPLICANT(S) FOR DO/EO/US

  Pierrick Jouet

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))

    a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).

    b. ☒ has been transmitted by the International Bureau.

    c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).

6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. ☒ A copy of the International Search Report (PCT/ISA/210). attached to Item 13

8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))

    a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).

    b. ☐ have been transmitted by the International Bureau.

    c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.

    d. ☒ have not been made and will not be made.

9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).

11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).

12. ☒ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98. with references attached

14. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

15. ☒ A FIRST preliminary amendment.

16. ☐ A SECOND or SUBSEQUENT preliminary amendment.

17. ☐ A substitute specification.

18. ☐ A change of power of attorney and/or address letter.

19. ☒ Certificate of Mailing by Express Mail   20. Return postcard receipt

20. ☒ Other items or information: **CERTIFICATE OF MAILING UNDER 37 CFR 1.10**

EL682441683US	January 30, 2001
"Express Mail" mailing no.	Date of Deposit

I hereby certify that this application is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Davida Fornarotto	_(signature)_
Typed or printed name of person mailing application	Signature of person mailing application

U.S. APPLICATION NO. (IF KNOWN SEE 37 CFR 09/744796	INTERNATIONAL APPLICATION NO. PCT/FR99/01568	ATTORNEY'S DOCKET NUMBER PF980052

21. The following fees are submitted:.	CALCULATIONS PTO USE ONLY

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO............$1000.00

☒ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO $860.00

☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $710.00

☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)............$690.00

☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)..........$100.00

JC## Rec'd PCT/PTO   3 0 JAN 2001

ENTER APPROPRIATE BASIC FEE AMOUNT =   860.00

Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	8 - 20 =	0	x $18.00	
Independent claims	1 - 3 =	0	x $80.00	
Multiple Dependent Claims (check if applicable).			☐	

TOTAL OF ABOVE CALCULATIONS =   860.00

Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) (check if applicable). ☐

SUBTOTAL =   860.00

Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +

TOTAL NATIONAL FEE =   860.00

Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) (check if applicable). ☐   40.00

TOTAL FEES ENCLOSED =   900.00

Amount to be: refunded	$
charged	$ 900.00

☐ A check in the amount of ___ to cover the above fees is enclosed.

☒ Please charge my Deposit Account No. 07-0832 in the amount of $900.00 to cover the above fees. A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 07-0832 A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Mr. Joseph S. Tripoli
THOMSON multimedia Licensing Inc.
Patent Department
PO Box 5312
Princeton, New Jersey 08540

Robert D Shedd
SIGNATURE

Robert D. Shedd
NAME

36,269
REGISTRATION NUMBER

January 30, 2001
DATE

SCANNED # 14

Item #
15

STATES PATENT AND TRADEMARK OFFICE

rick Jouet

Filed   :   Herewith

For   :   CLOCK RECOVERY METHOD IN DIGITAL SIGNAL
                     SAMPLING

PRELIMINARY AMENDMENT

Hon. Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Sir:

In the US national phase application of PCT/FR99/017685 filed herewith, please enter the following amendments:

IN THE TITLE:

Please amend the title of the application to read "CLOCK RECOVERY METHOD IN DIGITAL SIGNAL SAMPLING".

IN THE SPECIFICATION:

Please amend the specification as follows:

On Page 1, lines 1-2, please delete "METHOD OF CLOCK RECOVERY DURING THE SAMPLING OF SIGNALS OF DIGITAL TYPE" and insert --CLOCK RECOVERY METHOD IN DIGITAL SIGNAL SAMPLING--.

On Page 1, following the title, insert:

-- This application claims the benefit under 35 U.S.C. § 365 of International Application PCT/FR99/01768, filed July 20, 1999, which claims the benefit of French Application Serial No. 9809744, filed July 30 1998.--

IN THE CLAIMS:

Please amend the claims as follows:

1

1.(AMENDED) Method of clock recovery during the sampling of signals of digital type, the sampling clock being generated from a phase-lock loop or PLL [(1)] which multiplies a given frequency by an integer number or "division rank", the method comprising a step of comparing the relative position of the signals of digital type with respect to the sampling clock in such a way as to determine whether a chosen type of transitions of the sampling clock is in phase with the same type of transitions of signals of digital type:

• by formulating [(6)], over a period of the sampling clock, several zones, a zone corresponding to the chosen type of transitions,

• by analysing [(5)] the transitions of the signals of digital type with respect to the rising and falling transitions of the sampling clock,

• by aggregating in the corresponding zone the analysis results, and

• by determining [(10, 9)], as a function of the aggregates, whether or not a modification of the frequency and/or of the phase of the sampling clock needs to be carried out,

[characterized in that] wherein the results of the aggregations are utilized as follows:

a) all the information is in the zone corresponding to the chosen type of transitions, the signals of digital type are in phase and in frequency with the sampling clock;

b) the information is in two non-adjacent zones, there is a frequency error between the signals of digital type and the sampling clock;

c) the information is in two adjacent zones or in a single zone different from the zone corresponding to the chosen type of transitions, there is a phase error between the signals of digital type and the sampling clock.

2. (AMENDED)   Method according to Claim 1, [characterized in that] wherein the analysis step is preceded by a step of shaping the signals of digital type into logic signals.

3.(AMENDED) Method according to [either one of Claims 1 and 2, characterized in that] Claim 1, wherein the chosen type of transition is the falling transition.

4.(AMENDED) Method according to [any one of Claims 1 to 3, characterized in that] Claim 1, wherein four zones are formulated, with one zone corresponding to a rising

transition, one zone corresponding to a falling transition, one zone corresponding to a top porch and one zone corresponding to a bottom porch.

5.(AMENDED) Method according to [any one of Claims 1 to 4, characterized in that] Claim 1,wherein the analysis is carried out with the aid of two windows respectively corresponding to the rising and falling transitions of the sampling clock.

6.(AMENDED) Method according to Claim 1, [characterized in that] wherein the relative values of the information in two different zones or the value of the information in a zone different from the zone corresponding to the chosen type of transitions determine the sense and the amplitude of the phase correction or frequency correction to be applied to the sampling clock.

7.(AMENDED) Device for the implementation of the method according to [any one of Claims 1 to 6, characterized in that] Claim 1, wherein it comprises an erasable programmable electronic circuit receiving the signals of digital type as input as well as signals for determining the position of the various zones, the said erasable programmable electronic circuit delivering as output a phase error signal sent to a pulse width modulation circuit whose output acts on the PLL.

8.(AMENDED) Device according to Claim 7, [characterized in that] wherein the signals for determining the position of the various zones are obtained by a combinatorial logic

IN THE ABSTRACT:

Please add the following Abstract.

" The invention concerns a clock recovery method in digital signal sampling, the clock being generated from a phase-locking loop or PLL which multiples a given frequency by a whole number. Said method comprises a step which consists in comparing the relative position of the signals with respect to the clock so as to determine whether a selected type of the clock transitions is in phase with the same type of signal transitions by: producing over a clock period several zones, one zone corresponding to the selected type of transitions; analysing the signal transitions

relatively to the clock uplink or downlink transitions; cumulating in the corresponding zone the analysis results; determining on the basis of the accumulation whether the sampling clock frequency and/or phase needs to be modified or not. The invention is applicable to signals derived from graphics cards.

IN THE DRAWINGS:

Please replace the originally filed page 1 / 4, Figure 1 with the attached new page 1 / 4, Figure 1.

REMARKS

The title has been amended to conform with the translated title of the published application (WO 00/07324).

The specification has been amended to included the change in title and to include a reference to the priority applications.

The above amendments to the claims have been made to eliminate reference indicia, to eliminate the multiple dependencies and to meet the requirements of the United States.

To meet the requirements of the United States, the Abstract (as originally filed in the PCT application) is added.

Page 1 / 4, Figure 1 of the Drawings has been amended as per the International Preliminary Examination Report.

No fee is believed to have been incurred by virtue of this amendment. However if a fee is incurred on the basis of this amendment, please charge such fee against deposit account 07-0832

Respectfully submitted,
Pierrick Jouet

Robert D. Shedd, Attorney
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609/734-9517

THOMSON multimedia Licensing Inc.
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January 30, 2001

1.   Method of clock recovery during the sampling of
signals of digital type, the sampling clock being
5   generated from a phase-lock loop or PLL (1) which
multiplies a given frequency by an integer number or
"division rank", the method comprising a step of
comparing the relative position of the signals of
digital type with respect to the sampling clock in such
10   a way as to determine whether a chosen type of
transitions of the sampling clock is in phase with the
same type of transitions of signals of digital type:

•   by formulating (6), over a period of the
sampling clock, several zones, a zone corresponding to
15   the chosen type of transitions,

•   by analysing (5) the transitions of the signals
of digital type with respect to the rising and falling
transitions of the sampling clock,

•   by aggregating in the corresponding zone the
20   analysis results, and   .

•   by determining (10, 9), as a function of the
aggregates, whether or not a modification of the
frequency and/or of the phase of the sampling clock
needs to be carried out,
25   characterized in that the results of the aggregations
are utilized as follows:

a) all   the   information   is   in   the   zone
corresponding   to   the   chosen   type   of
transitions, the signals of digital type are in
30   phase and in frequency with the sampling clock;

b) the information is in two non-adjacent zones,
there is a frequency error between the signals
of digital type and the sampling clock;

c) the information is in two adjacent zones or in
35   a   single   zone   different   from   the   zone
corresponding   to   the   chosen   type   of
transitions, there is a phase error between the
signals of digital type and the sampling clock.

AMENDED SHEET

2.   Method according to Claim 1, characterized in that the analysis step is preceded by a step of shaping the signals of digital type into logic signals.

3.   Method according to either one of Claims 1 and 2, characterized in that the chosen type of transition is the falling transition.
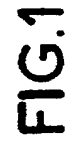
4.   Method according to any one of Claims 1 to 3, characterized in that four zones are formulated, with one zone corresponding to a rising transition, one zone corresponding to a falling transition, one zone corresponding to a top porch and one zone corresponding to a bottom porch.

5.   Method according to any one of Claims 1 to 4, characterized in that the analysis is carried out with the aid of two windows respectively corresponding to the rising and falling transitions of the sampling clock.

6.   Method according to Claim 1, characterized in that the relative values of the information in two different zones or the value of the information in a zone different from the zone corresponding to the chosen type of transitions determine the sense and the amplitude of the phase correction or frequency correction to be applied to the sampling clock.

7.   Device for the implementation of the method according to any one of Claims 1 to 6, characterized in that it comprises an erasable programmable electronic circuit receiving the signals of digital type as input as well as signals for determining the position of the various zones, the said erasable programmable electronic circuit delivering as output a phase error signal sent to a pulse width modulation circuit whose output acts on the PLL.

8.   Device according to Claim 7, characterized in that the signals for determining the position of the various zones are obtained by a combinatorial logic circuit processing the signal arising from the PLL.

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AMENDED SHEET

1/4

FIG.1

METHOD OF CLOCK RECOVERY DURING THE SAMPLING OF SIGNALS
OF DIGITAL TYPE

5   The present invention relates to a method of
clock recovery during the sampling of signals of
digital type, more particularly to a method making it
possible to recover the clock during the sampling of
video signals arising from a computer device such as a
graphics card.

10   The sampling of video signals arising from an
analogue source is well known. It uses the Shannon-
Nyquist theorem. According to this theorem, if the
passband of a signal is limited to a frequency domain
such as [0,Fmax], it is necessary and sufficient to

15   sample this signal at a minimum frequency of 2 × Fmax
in order to be capable of reconstructing it from these
samples. This constraint is manifested through the
introduction of low-pass filters whose purpose is to
limit the spectrum of the signals before sampling. In

20   this case, the phase of the clock signal is of no
importance in the sampling process. Indeed, one and the
same signal which is sampled by two clocks of the same
frequency but is phase shifted contains the same
information to within a constant delay.

25   Such is not the case when one needs to sample
video signals arising from a computer device, namely
signals of digital origin. Indeed, the spectrum of
these signals is very wide and they are intended to be
displayed with the highest possible resolution.

30   Accordingly, the passband should not be limited, since
there would be a loss of fineness. Now, if signals of
this type need to be injected into a device which
comprises a sampling stage, one is confronted with the
following problems:

35   •   If the incident signal is filtered so as to
limit its passband and satisfy the Nyquist criteria,
the response of the filter to signals of digital type
exhibiting steep transitions will give rise to over-

- 2 -

oscillations which are highly prejudicial to the sharpness of the characters.

•   If the incident signal is filtered only slightly so as to avoid over-oscillation, the

5   attenuation afforded to the frequency components will be insufficient to avoid likewise prejudicial spectral aliasing.

•   If the incident signal is sampled without prior filtering, it is imperative to adopt not only the exact

10   frequency which served to generate the signal, but also a sampling phase corresponding to the middle of each porch.

The problem is all the more complex since there is no predefined fixed standard in this area. Indeed,

15   in respect of the displaying of video signals arising from a graphics card, only the number of active pixels per line of the source and the number of active lines per image of the source are defined. Accordingly, the total number of pixels per line, the total number of

20   lines and the image frequency and pixel frequency are not standardized. Likewise, the phase of the first active pixel with respect to the edge of the synchronization clock is not defined, neither line-wise nor image-wise.

25   Accordingly, a purpose of the present invention is to propose a method making it possible automatically to recover the parameters of frequency and of phase of the sampling clock in the case of the sampling of signals of digital type, more particularly of video

30   signals arising from a device of computer type.

The present invention relies on the fact that in order to be correctly sampled, incoming information must be in phase with one of the edges, more particularly the falling edge of the sampling clock,

35   the realization of these criteria at various points of one and the same line implying a correct value of the frequency.

Accordingly, a subject of the present invention is a method of clock recovery during the sampling of signals of digital type, the sampling clock being generated from a phase-lock loop or PLL which multiplies a given frequency by an integer number or "division rank", characterized in that it comprises a step of comparing the relative position of the signals of digital type with respect to the sampling clock in such a way as to determine whether a chosen type of transition of the sampling clock is in phase with the same type of transition of the signals of digital type:

• by formulating, over a period of the sampling clock, several zones, a zone corresponding to the chosen type of transition,

• by analysing the transitions of the signals of digital type with respect to the rising and falling transitions of the sampling clock,

• by aggregating in the corresponding zone the analysis results, and

• by determining, as a function of the aggregates, whether or not a modification of the frequency and/or of the phase of the sampling clock needs to be carried out.

According to another characteristic of the present invention, the analysis step is preceded by a step of shaping the signals of digital type into logic signals.

Preferably, the chosen type of transition is the falling transition.

According to a preferred embodiment in order to carry out the analysis of the transitions, four zones are formulated, with one zone corresponding to a rising transition, one zone corresponding to a falling transition, one zone corresponding to a top porch and one zone corresponding to a bottom porch, the analysis being carried out with the aid of two windows respectively corresponding to the rising and falling transitions of the sampling clock.

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Preferably, the results of the aggregates are utilized as follows:

a) all the information is in the zone corresponding to the chosen type of

5
transition, the signals of digital type are in phase and in frequency with the sampling clock;

b) the information is in two non-adjacent zones, there is a frequency error

10
between the signals of digital type and the sampling clock;

c) the information is in two adjacent zones or in a single zone different from the zone corresponding to the chosen type of

15
transition, there is a phase error between the signals of digital type and the sampling clock.

The relative values of the information in two different zones or the value of

20
the information in a zone different from the zone corresponding to the chosen type of transition therefore determine the sense and the amplitude of the phase correction or frequency correction to be

25
applied to the sampling clock.

The present invention also relates to a device for implementing the abovementioned method, this device essentially comprising an erasable programmable electronic circuit receiving the signals of digital

30
type as input as well as a window-generating circuit sending signals determining the position of the various zones to the erasable programmable electronic circuit, the said erasable programmable electronic circuit delivering as output a phase error signal sent to a

35
pulse width modulation circuit whose output acts on the PLL.

Other characteristics and advantages of the present invention will become apparent upon the reading

hereinbelow of a preferred mode of implementation with
reference to the hereinappended drawings in which:

Figure 1 is a schematic of a device in
accordance with the present invention,

5   Figure 2 represents the various tests carried
out in accordance with the method of the present
invention,

Figure 3 represents a schematic of the erasable
programmable logic circuit or EPLD, and

10   Figure 4 is a representation of the state
machine making it possible to implement in the erasable
programmable logic circuit or EPLD the method of the
present invention.

To simplify the description in the figures, the
15 same elements carry the same references.

The circuit represented in Figure 1 makes it
possible to analyse the position of the incoming
information, namely of the signals of digital type DATA
IN with respect to the clock CK arising from the phase-
20 lock loop or PLL1. To implement this analysis, the
signals of digital type DATA IN are sent to a reception
circuit 2 comprising in a known manner an amplifier. At
the output of this circuit 2, the signals of digital
type are shaped so as to obtain logic signals, more
25 particularly signals of TTL type. The shaping circuits
more particularly comprise a differentiator 3
consisting in a known manner of a capacitor C3 and of a
resistor R3. The capacitor C3 is mounted in series
between the output of the reception circuit 2 and the
30 output of the differentiator 3, the resistor R3 being
mounted between the output point of the differentiator
3 and earth. The differentiator is followed by a
shaping circuit proper formed essentially of a
comparator COMP4 receiving on its positive input the
35 output from the differentiator 3 and on its negative
input a comparison voltage V_{thresh} fixed at a positive
voltage close to 0V. Moreover, to avoid untimely
triggering of the comparator in the presence of signals

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arising from the differentiator whose level is equal to V_{thresh}, the inverted output of the comparator COMP4 is looped back by way of a resistor R4 to the positive input of the said comparator. The logic signals DATA

5   arising from the shaping circuit 4 are sent to an analysis circuit or erasable programmable logic circuit EPLD5. This circuit will be described in detail hereinbelow.

Moreover, the phase-lock loop or PLL 1 receives

10 a synchronization signal H IN. This synchronization signal passes through a reception circuit 7 of known type essentially comprising an FET transistor T7 and a capacitor C7 mounted in parallel on the output of the said transistor. In this way, the signal H IN charges

15 the capacitor across the said transistor T7 and a signal as represented at 8 is obtained at output, with the rising edge of the signal, the image of the charge of the capacitor, having an exponential shape. This signal 8 is sent to the input of a shaping circuit 9

20 consisting of a comparator COMP9. This signal 8 is applied to the negative terminal of the comparator whilst the positive terminal receives a signal arising from a filtering circuit 10 which receives as input a PWM ("Pulse Width Modulation") signal the obtaining of

25 which will be explained later. Thus, a variation of the signal bound for the positive input of the comparator COMP9 makes it possible to delay the signal serving as reference to the PLL1 and thereby to modify the phase of the clock CK. The PLL1 is a conventional circuit

30 incorporating a phase comparator and a voltage-controlled oscillator or VCO. At the output of the PLL1 is provided a circuit 6 making it possible to formulate the analysis zones, namely the windows. This circuit could be integrated into the EPLD 5. The circuit 6 is a

35 circuit consisting of delay circuits D and of various logic gates making it possible to generate windows FEN1 and FEN2 in combinatorial logic from the clock CK and to thus produce the four analysis zones, namely zone 1

which corresponds to a top porch, zone 2 which
corresponds to a bottom porch, zone 3 which corresponds
to a rising transition and zone 4 which corresponds to
a falling transition, as represented in the top part of
5   Figure 2. In fact, the accuracy of the system will
depend on the width of the windows FEN1 and FEN2
centred about the rising and falling transitions. Thus,
the narrower the window FEN2, corresponding to the
falling transition, the more accurate the system will
10 be.

The clock recovery method in accordance with
the present invention therefore consists in analysing
the transitions of the signals of digital type DATA
with respect to the rising and falling transitions of
15 the clock CK. As mentioned hereinabove, this analysis
is carried out by using the windows FEN1 and FEN2 which
make it possible to determine analysis zones, namely
the zones 1, the zones 2, the zones 3 and the zones 4.
Thus, during a specified analysis time, the phase
20 information regarding the phase between the logic
signals DATA and the various zones is aggregated in the
various zones. At the end of the specified time, the
results of the aggregation are utilized so as to deduce
therefrom any possible phase correction and/or
25 frequency correction. The possible apportionments to
the various zones are represented in Figure 2. If all
the aggregated information is in zone 4, namely the
zone of the falling transition, as symbolized by AR4 in
Figure 2, from this one deduces that the signal CK is
30 in phase with the logic signals DATA and no action is
carried out on the phase. If information is only in
zone 1, namely the top-porch zone, as represented by
AR1 in Figure 2, one deduces from this that a phase
reduction must be carried out. Likewise, if information
35 is scheduled in zone 1 (AR1) and in zone 3 (DEP3) but
the level of cumulative total is attained in zone 1
(AR1). Such is the case also when information is
present in zone 1 and in zone 4 but the cumulative

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total is attained in zone 1 or information is present
in zone 1 and in zone 4 and the cumulative total is
attained in zone 4 or else information is present in
zone 3 and in zone 1 and the cumulative total is

5 attained in zone 3. This is symbolized by ARi for the
level of cumulative total attained in a zone and DEPi
for the presence of information in a zone.

Conversely, an increase in the phase shift will
be carried out when the following results of

10 aggregation are attained. The information is present
only in zone 2, namely the bottom-porch zone.
Information is present in zone 4 and in zone 2 but the
cumulative total is attained in zone 2. Information is
present in zone 2 and in zone 3, the level of

15 cumulative total being attained in zone 2. Information
is present in zone 4 and in zone 2, the level of
cumulative total being attained in zone 4. Information
is present only in zone 3 with a level of cumulative
total attained in this zone and information is present

20 in zone 2 and in zone 3 with the level of cumulative
total attained in zone 3.

An action on the frequency will be performed
when information is present in two non-adjacent zones.
Thus, as represented at the bottom of Figure 2,

25 information may be present in zone 1 and in zone 2
without attaining the level of cumulative total or
information may be present in zone 1 and in zone 2 with
a level of cumulative total attained in zone 2 or
information may be present in zone 1 and in zone 2 with

30 a level of cumulative total attained in zone 2. The
level of cumulative total can be attained both in zone
1 and in zone 2, the information may be present in zone
3 and in zone 4 without the level of cumulative total
attained. The information may be present in zone 3 and

35 in zone 4 with a level of cumulative total attained in
zone 4. Information may be present in zone 3 and in
zone 4 with a level of cumulative total attained in
zone 3 and information may be present in zone 3 and in

zone 4 with the level of cumulative total attained in
zones 3 and 4.

5   The method hereinabove may be implemented in a
programmable logic circuit EPLD such as represented in
Figure 3 by using a state machine whose symbolic
representation is given in Figure 4. The aggregation of
the phase information is performed in four counters
CPTZ1, CPTZ2, CPTZ3, CPTZ4, which aggregate the number
of transitions per zone. These counters receive as
10   input the signals FEN2 and FEN1, the clock signal CK
and the inverted clock signal CKB. They also receive
the logic signals DATA. Each counting is initialized
and authorized by the state S2 of the state machine.
This state is the state of initialization of the
15   signals ar and incf in the normal regime. In this
state, ar signifying the authorization of aggregation
of the information at the level of the counters
DECODAGEZ1, DECODAGEZ2, DECODAGEZ3, DECODAGEZ4 is at
zero, infc = 0 and signifies that the pulse which
20   serves to determine the frequency increment is reset to
0 and pwm_dec signifies that the state of the circuit
PWM_DEC is maintained in the previous state. The signal
ARi signifying that the level of cumulative total is
attained in a zone, is activated as soon as one of the
25   counters CPTZ1, CPTZ2, CPTZ3 and CPTZ4 attains a final
value thus authorizing the tests. The signal DEPi
signifying that information is present in a zone i will
be active if, during the analysis, the counter
associated with the relevant zone has left its initial
30   state. This analysis is carried out in the circuits
referenced DECODAGEZ1, DECODAGEZ2, DECODAGEZ3,
DECODAGEZ4. Subsequently, a test zone makes it possible
to carry out the tests mentioned with reference to
Figure 2, namely TEST4 maintaining the phase, TEST3
35   carrying out a reduction in the phase shift, TEST2
carrying out an increase in the phase shift and TEST1
involving an action on the frequency once the state ARi
is attained. Depending on the result, the processing

will be oriented either towards a phase action, or
towards a frequency action. Thus, as represented in
Figure 3, the output from TEST1 corresponding to the
fact that when a circuit more particularly a counter

5   DECODAGEZi has attained the aggregate level,
information is present in zones which are not adjacent,
passes through the state S6 of the state machine
corresponding to timeo = 1, incf = 1, pwm_dec = pwm =
init, this signifying that the frequency information is

10   false and the timeout is set and is sent to a counter
CPTINCF to carry out an action on the frequency later
on, whilst the outputs of TEST2, TEST3 and TEST4
through the states S5, S4, S3 respectively are sent to
a circuit PWM DEC making it possible to count up or

15   count down in respect of an action on the phase. More
specifically, the value arising from TEST2 signifying
that when a counter DECODAGEZi has attained the
aggregate level, information is present in adjacent
zones, is sent to the "up" counting input, the value

20   arising from TEST3 signifying that when a counter
DECODAGEZi has attained the aggregate level,
information is present in adjacent zones, is sent to
the "down" counting input whilst the value arising from
TEST4 signifying that when the counter DECODAGEZ4 has

25   attained the aggregate level, no information is present
in adjacent zones, does not modify the value of the
up/down counter PWM_DEC. Moreover, the up/down counter
PWM_DEC is loaded on its "load" input by the states S1
and S6 and is triggered by the information DATA, as

30   explained later on.
          In more detail, the various states Si of the
state machine represented in Figure 4 correspond to the
following states:
          S1: state of initialization of the state

35   machine. S1 is accessed by powering up the system.
          S2: state of initialization of the signals ar
and $incf$ in the normal regime. Each time the system
passes through S2, ar and $incf$ are reset to zero.

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S3: when the system is in this state, the phase and frequency information is correct. The timeout is set.

S4: when the system is in this state, the frequency information is correct but the phase information is not. It is necessary to reduce the phase shift. The timeout is set.

S5: when the system is in this state, the frequency information is correct but the phase information is not. It is therefore necessary to increase the phase shift. The timeout is set.

S6: when the system is in this state, the frequency information is false and the timeout is set.

S7: when the system is in this state, the signal *ar* is set to 1 and *incf* to 0. The counter pwm_dec[] is maintained in its previous state.

S8: when the system is in this state, the signal *ar* is set to 1 and *incf* to 0. The counter pwm_dec[] is maintained in its previous state. In fact, this state is redundant with S7 and can be eliminated.

In accordance with the present invention, the monitoring of the phase is carried out by using a pulse width modulation or PWM. The signal PWM-OUT generated by the EPLD circuit 5 possesses a variable duty ratio. A DC component is extracted from this signal by a low-pass filter such as the circuit 10 consisting in a known manner of a resistor R10 and of a capacitor C10. The result at the output of the filter 10 is therefore a DC voltage directly proportional to the duty ratio of the signal. Instead of a pulse width modulation circuit, it is also possible to use a serial digital/analogue converter. Thus, a modification of the duty ratio induces a modification of the overlap threshold of the sampling signal H IN and is manifested as a modification of the phase of the signal at the output of the PLL1. As represented in Figure 3, the PWM signal is generated with the aid of two counters, the up/down counter PWM_DEC and the counter PWM_CPT which

is a free counter counting between 0 and 768 for
example, and which is initialized by the clock CK. The
up/down counter PWM_DEC covers the range 0/255. It is
initialized on startup with the state S1 and each time
5   the state machine passes through the state S6. As
mentioned above, the activation of the states S4 or S5
respectively determines either an incrementation or a
decrementation of the previous value of the counter.
The switching rate of the counter is synchronous with
10 the DATA signals and its maximum period is the
cumulative total of the analysis and timeout times.
Passing through the state S3 causes the previous value
to be maintained and passing through the state S6
brings about the return to the initial value, i.e. a
15 duty ratio of 50%. This recentring makes it possible to
avoid a positioning towards the ends which would be
manifested by a state of instability, in particular
when the counter is positioned at 255 and an increment
takes it back to the 0 state. The signals arising from
20 the circuits PWM_DEC and PWM_CPT are sent as input to a
comparator COMP1 whose output is sent to a circuit T
which receives on its other input the output from a
decoding circuit DEC1 which sets the signal PWM_OUT to
the 1 level when the counter PWM_CPT attains the state
25 256. The signal PWM_OUT reverts to 0 when the following
conditions hold simultaneously, namely the MSB of the
counter PWM_CPT is equal to 1 and equality is achieved
between the 7 low-order bits of the counter PWM_CPT and
the counter PWM_DEC. The circuit T makes it possible to
30 effect a timeout of the signal PWM_OUT in such a way as
to have time to apply each modification to the phase
shifter.

In accordance with the present invention, the
frequency will be monitored by modifying the number of
35 points of the divider serving for the PLL1. In the EPLD
circuit 5, the management of the frequency is carried
out by using two counters CPT PLL and CPT INCF. The
counter CPT PLL covers, in the embodiment represented,

the range 0,1279 and moves with each transition of the
clock CK. It is loaded with the state S1. The counter
CPT INCF covers the range 0,127 in the embodiment of
the present invention. It is initialized on startup
5 with the state S1 and its rate of switching will be
synchronous with the DATA signal and its maximum period
will be the cumulative total of the analysis and
timeout times. As already mentioned, the counter CPT
INCF is incremented by a pulse INCA generated by the
10 activation of the state S6 arising from the TEST1.

In the present invention, the frequency search
follows a different principle from that of the phase
search. In the phase search, a kind of slaving is
carried out, whilst the frequency search is of
15 empirical type. The point of departure is a value
corresponding to the minimum of the range of capture.
The counter CPT INCF is incremented until the phase
criteria are satisfied. Moreover, the counter CPT PLL
is reset to zero when the following conditions are
20 realized: the four MSBs of the counter CPT PLL are
equal to "1000", equality is achieved between the 6
low-order bits of the counter CPT PLL and the counter
CPT INCF, the latter condition being satisfied with
each cycle of the counter PWM CPT. Just as for the
25 counter PWM_DEC, each modification of the state of the
counter CPT INCF is retained for a minimum time
corresponding to the timeout time, this therefore
making it possible to apply each modification to the
divider. Moreover, as represented in Figure 3, the
30 output from the counter CPT PLL is sent to the input of
a decoding circuit DEC2 which also receives as input
the clock CK and to the input of a comparator COMP2,
which on its other input receives the output from the
circuit CPT INCF in such a way as to carry out the
35 abovementioned comparison operations. The comparator
COMP2 also receives the clock CK. The output from the
comparator COMP2 is sent to the inverted input of the
counter CPT PLL. Moreover, the output of the decoding

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circuit DEC2 gives the signal H LOCK, the PLL
comparison signal, which passes to the level when the
counter CPT PLL attains the 0.state. The recurrence of
this signal is directly related to the duration of a
5   cycle of the counter CPT PLL. Moreover, the EPLD
circuit of Figure 3 comprises circuits making it
possible to generate the state S8. The state S8 makes
it possible to return to S2 when the timeout has
elapsed, as represented in Figure 4. For this state,
10 the clock information H, at the input of the EPLD
circuit, is sent to an integrator 11 giving a signal FH
as output. This signal is sent to a timeout circuit
which is initially loaded with the states S3, S4, S5,
S6. The output from the timeout signal is sent to a
15 decoding circuit DEC3 which also receives as input the
clock CK. The output of the decoding circuit is sent to
a D flip-flop switched by the signal DATA CK and,
additionally, the output of .the decoding circuit is
looped back to the input of the timeout circuit.

20   Various modifications and improvements may be
made to the system described above. Thus, · the
authorization of the test depends on the states ARi
obtained when one of the aggregating counters attains
the value VAL END which is fixed for example at the
25 value 768. In this case, it is possible to determine
the lock-on time of the system. This time is given by
the following equation:

$$T = (F + P) \times ((\Sigma T_D) + 2 \times 10^{-3})$$

in which F represents the number of increments
30 required to obtain the correct frequency and P
represents the number of increments required to obtain
the correct phase.

ΣT_D represents the time required to acquire the
768 data.

35   In fact the maximum convergence time will be
attained when there is just one point per image. For an
image frequency of 50 Hz and for a point frequency
lying at the maximum of the frequency and phase

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compensation span, the time T is equal to 72 minutes.
This time may be greatly decreased by adapting the
value VAL END as a function of the input bit rate,
namely by counting the events during an image.

5   Moreover, in the presence of just one point per image,
it will be possible to respect the phase convergence
criteria, even though the frequency is wrong. For
better convergence, a simple solution consists in using
the rising edges and also the falling edges of the

10   information. In this case, the accuracy is dependent on
the width of the pulse and hence on the line-wise
position of the events.

        Moreover, by detection of standard, namely by
counting the number of lines per image, it is possible

15   to preset the counter CPT PLL to an initial value such
that the frequency obtained is at the bottom limit of
the target compensation span. This operation will
therefore make it possible to optimize the speed of
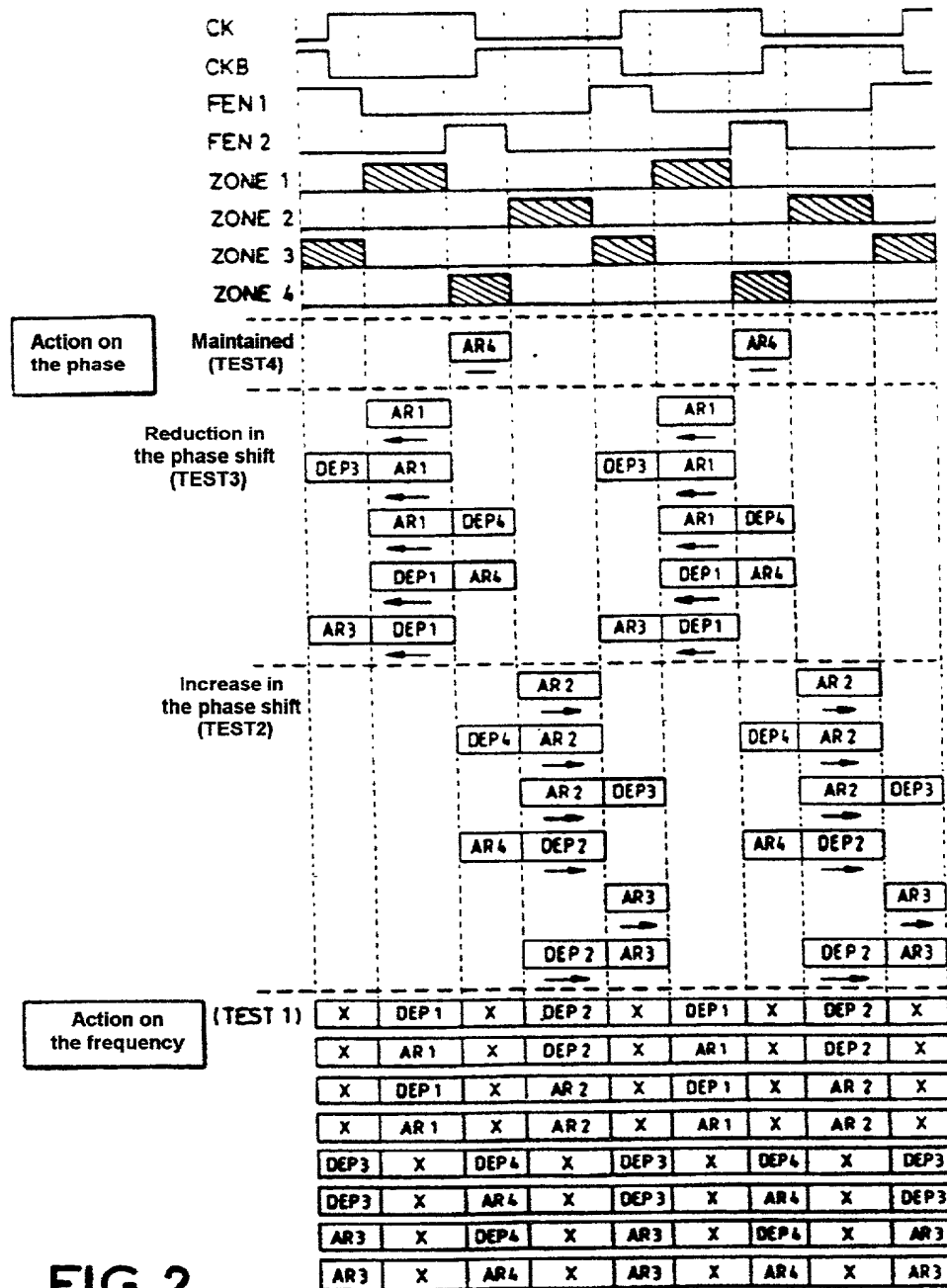convergence and to limit the phenomena of under- or

20   over-sampling.

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FIG.1

CK

CKB

FEN 1

FEN 2

ZONE 1

ZONE 2

ZONE 3

ZONE 4

| Action on the phase | Maintained (TEST4) | | AR4 | | | | AR4 | |

Reduction in the phase shift (TEST3)

	AR1				AR1	
DEP3	AR1			DEP3	AR1	
	AR1	DEP4			AR1	DEP4
	DEP1	AR4			DEP1	AR4
AR3	DEP1			AR3	DEP1	

Increase in the phase shift (TEST2)

	AR2				AR2	
DEP4	AR2			DEP4	AR2	
	AR2	DEP3			AR2	DEP3
	AR4	DEP2			AR4	DEP2
	AR3				AR3	
	DEP2	AR3			DEP2	AR3

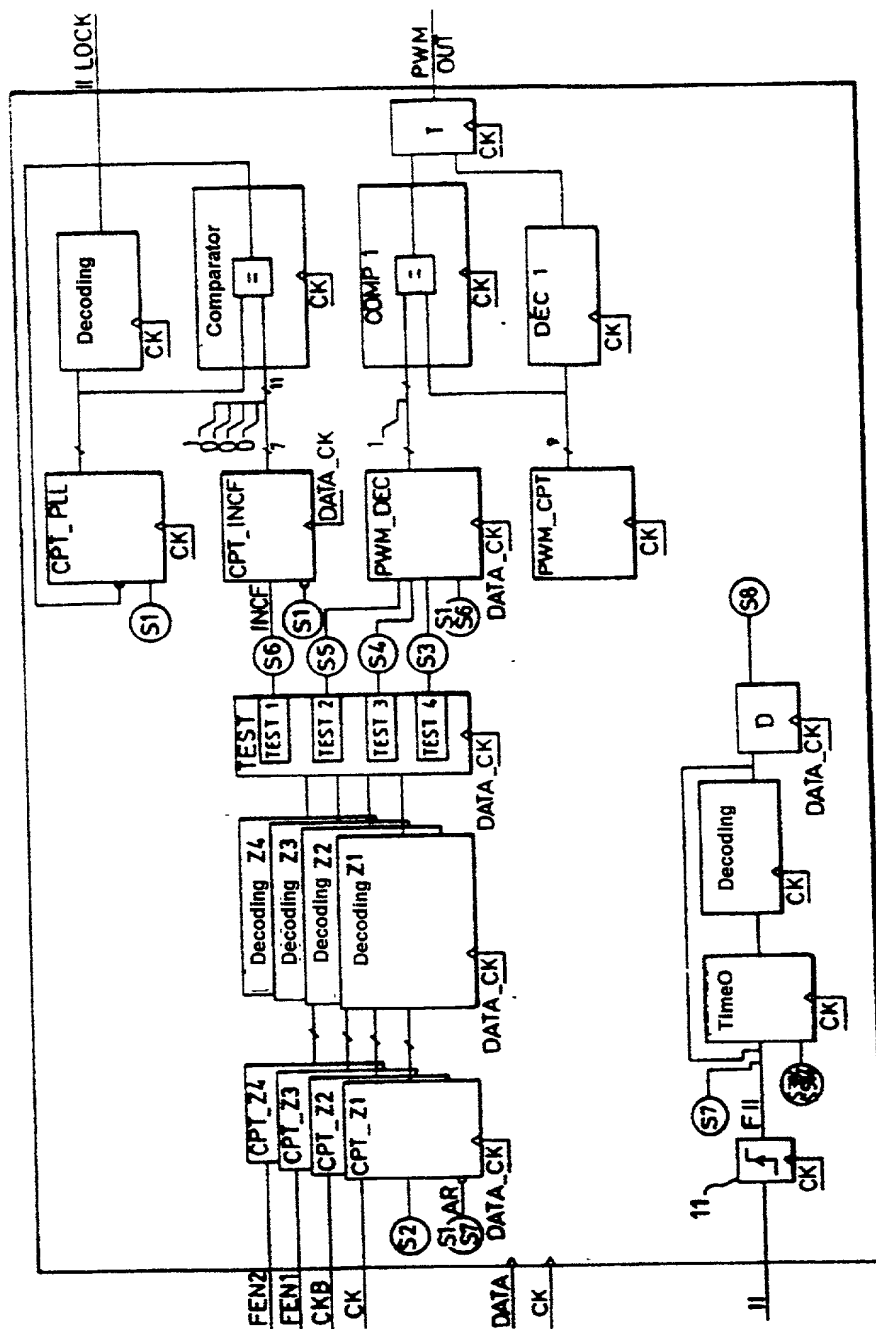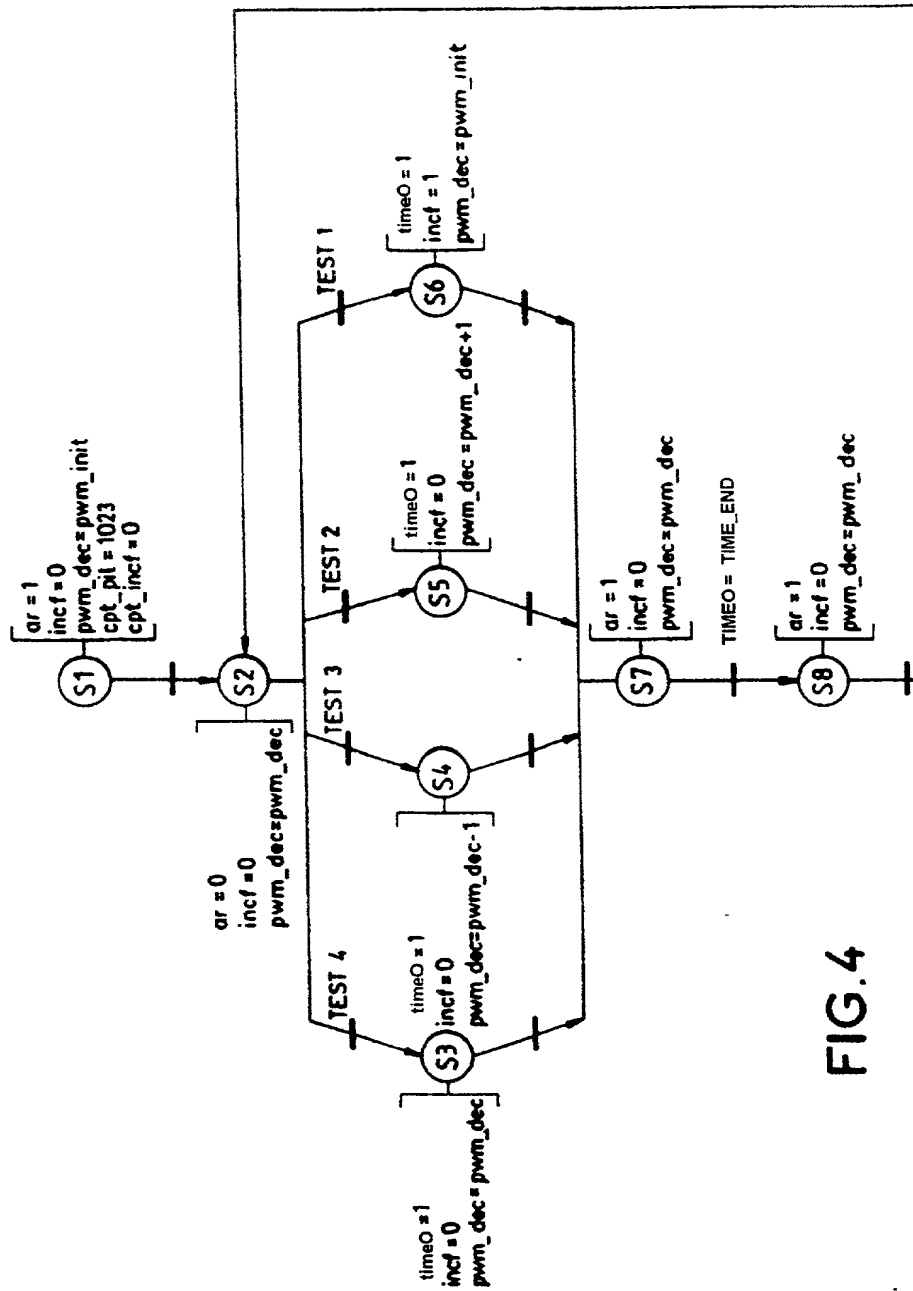| Action on the frequency	(TEST 1)	X	DEP1	X	DEP2	X	DEP1	X	DEP2	X
		X	AR1	X	DEP2	X	AR1	X	DEP2	X
		X	DEP1	X	AR2	X	DEP1	X	AR2	X
		X	AR1	X	AR2	X	AR1	X	AR2	X
		DEP3	X	DEP4	X	DEP3	X	DEP4	X	DEP3
		DEP3	X	AR4	X	DEP3	X	AR4	X	DEP3
		AR3	X	DEP4	X	AR3	X	DEP4	X	AR3
		AR3	X	AR4	X	AR3	X	AR4	X	AR3

FIG.2

FIG.3

FIG.4

DECLARATION FOR UNITED STATES PATENT APPLICATION, POWER OF ATTORNEY, DESIGNATION OF CORRESPONDENCE ADDRESS

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

"METHOD OF CLOCK RECOVERY DURING THE SAMPLING OF SIGNALS OF DIGITAL TYPE"

the specification of which
(CHECK ONE)   ( )   is attached hereto.
                 (xx)   was filed on July 20, 1999, Application Serial. No. PCT/FR99/01768 and was amended on

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 CFR 1.56(a).

I hereby claim foreign priority benefits under 35 USC 119 of any foreign application(s) for patent, utility model, design or inventor's certificate having a filing date before that of the application(s) on which priority is claimed:

| Prior Foreign Application(s) | | | Priority Claimed | |
Number	Country	Date Filed	Yes	No
9809744	FR	July 30, 1998	xx	

I hereby claim the benefit under 35 USC 120 of any US Application(s) listed below, and, insofar as the subject matter of each of the claims of this Application is not disclosed in the prior US application in the manner provided by the first paragraph of 35 USC 112, I acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 CFR 1.56(a).

Serial No.: _____   Filed: _____

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that wilful false statements and the like so made are punishable by fine or imprisonment, or both, under of 18 USC 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Joseph S. Tripoli (Reg. No. 26,040), Dennis H. Irlbeck (Reg. No. 26372), Joseph J. Laks (Reg. No. 27,914), Eric Herrmann (Reg. No. 29,169) Telephone: (609) 734-9754

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